REMARKS

Claims 9, 11, 12 and 16-25 are pending in the present application, were examined, and stand rejected. In response, no claims are amended, no claims are cancelled and no claims are added. Applicant respectfully requests reconsideration of pending Claims 9, 11, 12 and 16-25 in view of at least the following remarks. Reconsideration and withdrawal of the rejections of record are requested in view of such amendments and the following discussion.

I. Claims Rejected Under 35 U.S.C. §102

The Examiner has rejected Claim 23 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,223,258 issued to Palanca et al. ("Palanca"). Applicant respectfully traverses this rejection.

Regarding Claim 23, Claim 23 recites the following claim features, which are neither disclosed, taught nor suggested by Palanca:

> at least two memory modules, each memory module including:
> at least one memory device, and
> a data cache coupled to an eviction buffer, both coupled to the memory device. (Emphasis added.)

According to the Examiner:

> Palanca discloses a system memory (100, figure 1) comprising at least two memory modules (110_1 through 110p, figure 1), each module including at least one memory device (215, figure 3) and a data cache (320, figure 3) coupled to the an eviction buffer (340, figure 3), both coupled to the memory device (col. 3 lines 64 through col. 4 line 61 and col. 9 lines 52-56). (pg. 2, ¶3 of the Office Action mailed June 27, 2006.)

Applicant respectfully disagrees with the Examiner's contention that Palanca discloses the system memory, as recited by Claim 23. To anticipate the features of Claim 23, the Examiner relies on computer system 100, as shown in FIG. 1 of Palanca. According to the Examiner, computer system 100, which comprises one or more central processing units 110_1 through 110p, discloses a system memory, where CPUs 110_1 through 110p disclose the at least two memory modules recited by Claim 23. Applicant is unable to discern how a computer system 100 discloses a system memory or how the multiple CPUs of such system disclose the at least two memory modules, as recited by Claim 23.

As further indicated by the Examiner, reorder buffers & register file 215, writeback buffer 340 (*see*, FIG. 3) and LI cache 320 disclose the memory device, data cache and eviction buffer, as recited by Claim 23, which are both coupled to the memory device. According to the Examiner, such features of Claim 23 are disclosed at col. 3, line 64 through col. 4, line 61 and col. 9, lines 52-56 of Palanca. Applicant respectfully disagrees.

As mandated by case law, Applicant respectfully asserts that the Patent Office has failed to adequately set forth a *prima facie* rejection under 35 U.S.C. §102(b). "Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Lindemann Maschinenfabrik v. American Hoist & Derrick ("Lindemann"), 730 F.2d 452, 1458 (Fed. Cir. 1994) (emphasis added). Additionally, each and every element of the claim must be exactly disclosed in the anticipatory reference. Titanium Metals Corp. of American v. Banner ("Banner Titanium"), 778 F.2d 775, 777 (Fed. Cir. 1985).

Here, the Examiner relies on the computer system 100, as shown in FIG. 1 of Palanca, to disclose the system memory, as recited by Claim 23. Furthermore, the Examiner relies on CPUs 110_1 through 110p to teach the at least two memory modules of the system memory recited by Claim 23. Although CPUs 110_1 through 110p, as disclosed by Palanca, each include L1 cache 320, as shown in FIG. 3, the reorder buffers and register file 215 of processor core 208, as shown in FIG. 3, neither teach nor suggest the at least one memory device, as recited by Claim 23.

Applicant respectfully submits that the reorder buffers & register file 215, as illustrated in FIG. 3 of Palanca, and as known to those skilled in the art, are utilized to enable out-of-order execution, as referred to by Palanca. As indicated by Palanca:

> All references made to the reorder buffer and/or register file will be designated by numeral 215 even though they are separate logical units within the logical block 215. The register file includes a plurality of general purpose registers. (col. 3, lines 43-47.) (Emphasis added.)

Regarding the reorder buffer referred to by the Examiner, the functionality of such reorder buffer is defined by Palanca as follows:

> The reorder buffer 215 keeps a copy of the instructions in program order. Each entry in the reorder buffer, which corresponds to a micro-instruction, includes a control field with one bit being a write-back data valid bit. The write-back data valid bit indicates whether an instruction is ready to

be retired. The reorder buffer 215 retries the instruction when the instruction has its write-back data valid bit set and when all previous instructions in the reorder buffer have been retired (i.e., in-order retirement). (col. 6, lines 39-48.) (Emphasis added.)

Accordingly, the reorder buffers & register file 215, as taught by Palanca, include a plurality of registers as the register file, while the reorder buffer is provided to keep instructions in program order. Accordingly, based on such passages, and as taught by Palanca, the reorder buffers & register file 215 cannot disclose, teach or suggest a memory device, as recited by Claim 23.

Accordingly, for at least the reasons indicated above, Applicant respectfully submits that the Examiner is prohibited from relying on Palanca as an anticipatory reference, since Palanca fails to exactly disclose each and every element recited by Claim 23, and specifically, reorder buffers & register file 215, as shown in FIG. 3, of Palanca, fail to exactly disclose, teach or suggest the memory device recited by Claim 23. Banner Titanium, supra.

Consequently, Applicant respectfully submits that the Examiner fails to establish a *prima facie* case of anticipation with Palanca as an anticipatory reference, since the Examiner fails to illustrate that the single prior art reference disclosure of Palanca includes the presence of each and every element recited by Claim 23. Lindemann, supra.

Therefore, for at least the reasons provided above, Claim 23 is patentable over Palanca, as well as the references of record. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §102(b) rejection of Claim 23.

II. Claims Rejected Under 35 U.S.C. §103

The Examiner has rejected Claims 20-22 and 24-25 under 35 U.S.C. §103(a) as being unpatentable over Palanca in view of U.S. Patent No. 5,526,510 issued to Akkary et al. ("Akkary"). Applicant respectfully traverses this rejection.

Regarding Claim 20, Claim 20 recites a memory module, which includes the following claim features, which are neither taught nor suggested by the combination of Palanca in view of Akkary:

at least one memory device; and

a data cache coupled to an eviction buffer, both coupled to the memory device, the data cache controlled by a plurality of commands delivered by a memory controller over a memory bus,

the memory module to receive a write-back command, the write-back command to cause a previous line of data, evicted from the data cache and stored within the eviction buffer, to be written out of the eviction buffer to the memory device. (Emphasis added.)

As indicated above with regard to the §102(b) rejection of Claim 23, reorder buffers & register file 215 of processor core 208, as shown in FIG. 3 of Palanca, are defined by Palanca as follows: The register file 215 includes a plurality of general purpose registers (*see*, col. 3, lines 46-47), whereas the reorder buffer 215 keeps a copy of the instructions in program order and reorder buffer 215 retries the instruction when the instruction has its write-back data valid bit set and when all previous instructions in the reorder buffer have been retired (i.e., in-order retirement) (*see*, col. 6, lines 39-48).

Based on such definitions of reorder buffers & register file 215 of processor core 208, as shown in FIG. 3 of Palanca, Applicant respectfully submits that reorder buffers & register files 215 do not disclose, teach nor suggest a memory device of the memory module recited by Claim 20.

Regarding the Examiner's citing of Akkary, assuming Akkary taught the features performed by the memory module in response to a writeback command, as recited by Claim 20, modification of Palanca to cause the previous line of data, evicted from the data cache and stored within the eviction buffer, to be written out of the eviction buffer to the memory device, as recited by Claim 23, may result in data stored within writeback buffer 340 to be written out of writeback buffer 340 to reorder buffers & register file 215. However, for at least the reasons indicated above, reorder buffers & register file 215 do not represent a memory device from which data evicted from L1 cache 320 would be stored. (*See*, Fig. 3 of Palanca.) Furthermore, as taught by Palanca:

Continuing to refer to FIG. 3, the WBB 340 is used to write a line of data that is in the M state, which as been evicted from the L1 cache 320, to external memory 140. (col. 4, lines 29-31.) (Emphasis added.)

As mandated by case law, to establish a *prima facie* case of obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

Here, Palanca fails to teach or suggest a memory module including at least one memory device, which is coupled to both a data cache and an eviction buffer, as recited by Claim 20. Furthermore, the Examiner's citing of Akkary fails to rectify the deficiencies of Palanca in teaching the data cache and eviction buffer coupled to the memory device of the memory module recited by Claim 20.

Consequently, Applicant respectfully submits that the prior art references of Palanca in view of Akkary fail to teach or suggest all claim features recited by Claim 20, as required to establish *prima facie* obviousness.

Furthermore, since the writeback cache 340, as taught by Palanca, is used to write modified, evicted data from L1 cache 320 to external memory 140, one skilled in the art would not modify, and could not modify Palanca, as taught by Akkary, to write data from write buffer 340 to reorder buffers & register file 215 taught by Palanca. Consequently, Applicant respectfully submits that the combined teachings of Palanca in view of Akkary would not have suggested the claimed subject matter to one of ordinary skill in the art.

Therefore, Applicant respectfully submits that Claim 20 is patentable over the combination of Palanca in view of Akkary. Id. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 20.

Regarding Claims 21 and 22, Claims 21 and 22, based on their dependency from Claim 20, are also patentable over the combination of Palanca in view of Akkary. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 21 and 22.

Regarding Claims 24 and 25, Claims 24 and 25, based on their dependency from Claim 23, would also be patentable over the combination of Palanca in view of Akkary, since Akkary fails to rectify the deficiencies of Palanca in teaching or suggesting the system memory recited by Claim 20. Therefore, for at least the reasons provided above, Applicant respectfully submits that Claims 24 and 25, based on their dependency from Claim 23, are also patentable over the combination of Palanca in view of Akkary. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 24 and 25.

The Examiner has rejected Claims 9 and 11-12 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,378,049 issued to Stracovsky et al. ("Stracovsky") in view of Palanca and Akkary. Applicant respectfully traverses this rejection.

Regarding Claim 9, Claim 9 recites a memory module including the following features, which are neither disclosed, taught nor suggested by the combination of Stracovsky in view of Palanca and further in view of Akkary:

> at least one memory device, and
> a data cache coupled to an eviction buffer, both coupled to the memory device, the data cache controlled by a plurality of commands delivered by the memory controller, the memory controller writing a current line of data to the data cache, the memory controller to further instruct the data cache to evict a previous line of data from the data cache into the eviction buffer. (Emphasis added.)

Applicant respectfully submits that the above-recited features of Claim 9 regarding a memory module including at least one memory device coupled to both a data cache and an eviction buffer are analogous to the above-recited features of Claim 23. Accordingly, Applicant's arguments provided above with regard to the §103(a) rejection of Claim 20 apply to the Examiner's §103(a) rejection of Claim 9.

Hence, for at least the reasons indicated above, Palanca does not teach a memory module including at least one memory device and a data cache coupled to an eviction buffer, both coupled to the memory device. As previously indicated, the Examiner has incorrectly interpreted reorder buffers & register file 215 (*see*, FIG. 3) as a memory device, as recited by Claim 9.

Consequently, Applicant respectfully submits that the combination of Stracovsky in view of Palanca and further in view of Akkary, cannot teach all claim features recited by Claim 9, as required to establish a *prima facie* case of anticipation. In re Royka, supra. Therefore, for at least the reasons provided above, Applicant respectfully submits that Claim 9 is patentable over the prior art combination of Stracovsky in view of Palanca and further in view of Akkary.

Hence, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 9, as well as the §103(a) rejection of Claims 11-12, which based on their dependency from Claim 9, are also patentable over the combination of Stracovsky in view of Palanca and further in view of Akkary.

The Examiner has rejected Claims 16-19 under 35 U.S.C. §103(a) as being unpatentable over Stracovsky in view of Akkary. Applicant respectfully traverses this rejection.

Regarding Claim 16, Claim 16 recites the following claim features, which are neither disclosed nor suggested by the combination of Stracovsky in view of Akkary:

> an array of tag address storage locations; and
> a command sequencer and serializer unit coupled to the array of tag address storage locations, the command sequencer and serializer unit to control a data cache and an eviction buffer located on at least one memory module of a system memory, the command sequencer and serializer to deliver a writeback command to the eviction buffer associated with the memory module, the writeback command to cause a previous line of data evicted from the data cache and stored in the eviction buffer, to be written out to a memory device of the memory module. (Emphasis added.)

As recited by Claim 16, issuance of the writeback command to the eviction buffer associated with the memory module causes a previous line of data, evicted from the data cache and stored in the eviction buffer, to be written out to a memory device of the memory module. Applicant respectfully disagrees with the Examiner's contention that one of ordinary skill in the art would modify the write buffer 314 of Stracovsky, as disclosed by Akkary.

As correctly noted by the Examiner, Stracovsky fails to teach or suggest that the command sequencer and serializer unit controls the data cache and an eviction buffer located on at least one memory module of the system memory. (*See*, pg. 2, ¶1 of the Office Action mailed March 27, 2006.) As a result, the Examiner cites Akkary. As indicated by the Examiner:

> Akkary teaches in a data cache system comprising a plurality of cache banks (318, figure 2) and a write back buffer (322, figure 2) both coupled to the system memory via a system bus (308, figure 2) to perform memory operation in responds to an instruction from a central processing unit, wherein the write back buffer is capable of temporary storing the eviction entry from the cache bank, and further write back to a main memory such that a pervious line of data evicted from the data cache and stored within the write back buffer is written out of the write back buffer to the main memory (col. 6 lines 11-20 and lines 34-67.) [sic] (*See*, pg. 7, ¶1 of the Office Action mailed March 27, 2006.)

As indicated by the Examiner, cache banks 318 and writeback buffer 322 of FIG. 2 of Akkary are both coupled to system memory via system bus 308, as shown in FIG. 2. Applicant respectfully disagrees with the Examiner's contention.

As shown in FIG. 2 of Akkary, data cache banks 318 are coupled to CPU bus 316, fill buffer 320 and writeback buffer 322. In addition, writeback buffer 322 is coupled to system bus 308 to which main memory 310 is coupled.

Accordingly, as shown in FIG. 2 and as taught by Akkary, data cache banks 318 are not coupled to main memory 310. Furthermore, as recited by Claim 16, the data cache and eviction buffer are located on at least one memory module of a system memory. Applicant respectfully submits that neither the data cache banks 318 nor writeback buffer 322 are located on at least one memory module of system (main) memory 318, as shown in FIG. 2 of Akkary.

As mandated by case law, "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970.) Here, Applicant respectfully submits that the Examiner has failed to consider the following wording of Claim 16:

> a data cache and an eviction buffer located on at least one memory module of a system memory.

Applicant respectfully submits that Akkary teaches a data cache unit 314, as shown in FIG. 2, which includes data cache banks 318, which are coupled between fill buffer 320 and write buffer 322. As shown in FIG. 2, data cache banks may be coupled to a CPU bus 316, but are not coupled to a system bus 308, which couples main memory to fill buffer 320 and writeback buffer 322. Consequently, Applicant respectfully submits that the prior art combination of Stracovsky in view of Akkary, fails to at least teach or suggest a data cache and an eviction buffer located on at least one memory module of the system memory, as recited by Claim 16.

Therefore, Applicant respectfully submits that the Examiner's failure to consider all wording of Claim 16 prohibits the Examiner from establishing a *prima facie* case of obviousness of Claim 16, with prior art references of Stracovsky in view of Akkary, since such prior art combination fails to teach or suggest all claim limitations recited by Claim 16. In re Royka, supra.

Hence, Applicant respectfully submits that Claim 16 is patentable over the combination of Stracovsky in view of Akkary. Id. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 16.

Regarding Claims 17-19, Claims 17-19, based on their dependency from Claim 16, are also patentable over the prior art combination of Stracovsky in view of Akkary. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 17-19.

CONCLUSION

In view of the foregoing, it is submitted that Claims 9, 11, 12 and 16-25 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
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Dated: June 26, 2006

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CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on June 26, 2006

Marilyn Bass June 26 2006